Office Action Summary	Application No.	Applicant(s)	
	10/625,954	FAGERNESS ET AL.	
	Examiner	Art Unit	
	ROBERT C. SCHEIBEL	2467	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 November 2010*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____
4) ☒ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

- This action is in response to the Decision on Appeal mailed 11/26/2010.
- The rejection of claims 1-15 under 35 U.S.C. 103(a) was sustained and the rejection is maintained herein.
- The rejection of claims 16-19 under 35 U.S.C. 102(b) was not sustained. However upon a subsequent search, another reference disclosing the missing limitation was found. As such, claims 16-19 are rejected under 35 U.S.C. 103(a).

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

3. Claims **1-3 and 5-15** are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 5,414,701 to Shtayer, et al in view of U.S. Patent 6,356,552 to Foglar.

Regarding claims **1 and 11**, Shtayer discloses a method and system for determining a control block index for a data cell received by a network processor coupled to an ATM network comprising (see figures 3 and 5): receiving a data cell at a port, the data cell having a virtual path identifier and a virtual channel identifier (see figure 1 and lines 36-39 of column 4); determining a port number for the port (the PHY/LINK Id; see lines 36-40 of column 5, for example); employing bits of at least one of the virtual path identifier, the virtual channel identifier and the port number to create a first address (the PHY/LINK Id is used as the first address; see lines 36-40 of column 5); employing the first address to access a first memory and to obtain a first entry from the first memory (the entry in the Link Table of Figure 3), the first entry specifying: a first base memory address (the VP POINTER element of this entry); a number of bits of the virtual path identifier to use in the control block index (the VP_MASK field, as indicated in figure 4, indicates the number of VPI bits to be used). These sections of Shtayer also disclose the analogous limitations of claim 11.

However, Shtayer does not disclose expressly the limitation that the first entry specifies a number of bits of the port number to use in the control block index and a number of bits of the virtual channel identifier to use in the control block index; or the limitation of employing the first base memory address and the number of bits of the port number, virtual path identifier-and virtual channel identifier specified by the first entry to create a control block index for the data cell.

However, Foglar does disclose these limitations. Specifically, Foglar discloses a number of bits of the port number to use in the control block index (P bits; see figure 1); a number of bits of the virtual path identifier to use in the control block index (14-M bits; see figure 1); and a number of bits of the virtual channel identifier to use in the control block index (M-P bits; see figure 1). Foglar also discloses the limitation of employing the first base memory address and the number of bits of the port number, virtual path identifier-and virtual channel identifier specified by the first entry to create the control block index for the data cell (this is disclosed in the generation of the 14-bit LCI index throughout – see Figure 1, for example). Shtayer and Foglar are analogous art because they are from the same field of endeavor of ATM switching. At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify Shtayer to compress the multistage method of Shtayer (see Figure 3) to a single stage LCI generation method like that of Foglar. The motivation for doing so would have been to reduce the hardware complexity (and thus cost) required by the multistage scheme like Shtayer as suggested by Foglar in the background section – see lines 23-30 of column 3. Therefore, it would have been obvious to combine Foglar with Shtayer for the benefit of reducing hardware complexity (and thus cost) to obtain the invention as specified in claims 1 and 11.

Regarding claim **2**, the above combination clearly discloses the limitation that employing bits of at least one of the virtual path identifier, the virtual channel identifier and the port number to create the first address comprises employing bits of at least one of the virtual path identifier and the port number to create the first address as shown in Figure 1 of Foglar. Clearly, the VPI and port number are used in the creation of the LCI.

Regarding claims **3 and 12**, Shtayer discloses the limitation that the first memory is an on-chip memory of the network processor throughout – see figures 2 and 3, for example, which describe the link table as internal.

Regarding claims **5 and 13**, Shtayer does not disclose expressly the limitations of these claims. However, Foglar discloses the limitations that employing the first base memory address and the number of bits of the port number, virtual path identifier and virtual channel identifier specified by the first entry to create the control block index for the data cell comprises: selecting the number of bits of the port number specified by the first entry (see figure 1 – the P pits of port number PN are selected); selecting the number of bits of the virtual path identifier specified by the first entry (see figure 1 – the 14-M bits of the VPI are selected); selecting the number of bits of the virtual channel identifier specified by the first entry (see figure 1 – the M-P bits of the VCI are selected); catenating any selected bits (see lines 1-5 of column 6); and adding the catenated selected bits to the first base memory address (this is well known and taught in Shtayer (lines 22-25 of column 5); it is also clearly the intent of Foglar as the 14 bit LCI is intended to be able to identify 16 K connections (see lines 32-35 of column 5) and this is not possible unless the LCI is an offset from a base address (unless all 16 K addresses are stored at physical memory address zero which is impractical)). Shtayer and Foglar are analogous art because they are from the same field of endeavor of ATM switching. At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify Shtayer to compress the multistage method of Shtayer (see Figure 3) to a single stage LCI generation method like that of Foglar.

The motivation for doing so would have been to reduce the hardware complexity (and thus cost) required by the multistage scheme like Shtayer as suggested by Foglar in the background section – see lines 23-30 of column 3. Therefore, it would have been obvious to combine Foglar with Shtayer for the benefit of reducing hardware complexity (and thus cost) to obtain the invention as specified in claims 5 and 13.

Regarding claims **6 and 14**, the above combination of Shtayer and Foglar does not disclose expressly the limitations of shifting the control block index; and adding the shifted control block index to a main system memory base offset so as to generate a control block memory address. However, this would have been obvious to one of ordinary skill in the art and necessary for the above combination. In order for the above mentioned LCI (14 bits) to access 16 K entries where the entries are larger than one byte in size, the offset will need to be shifted by one or more bits prior to being added to the base address in order to properly identify the location in memory. At the time of the invention, it would have been obvious to one of ordinary skill in the art to explicitly perform this shifting of the index. The motivation for doing so would have been to allow the combination of Shtayer and Foglar to properly locate a memory entry of larger than one byte using the LCI index. Therefore, it would have been obvious to modify the combination of Shtayer and Foglar for the benefit of storing more information than a single byte per connection to obtain the invention as specified in claims 6 and 14.

Regarding claim **7**, Shtayer discloses the limitation of employing the control block memory address to obtain a control block from a main system memory in Figure 2 which shows

that the link table is internal memory (to the chip); the other tables are thus clearly stored in external or main memory and thus the control block address is used to obtain the control block from main memory.

Regarding claim **8**, the combination of Shtayer and Foglar as described above discloses all limitations of parent claim 5. This combination does not explicitly disclose the limitation of this claim. However, Foglar discloses the limitation of verifying that non-selected port number, virtual path identifier and virtual channel identifier bits are zeroed in the passage from line 59 of column 8 through line 4 of column 9. Shtayer and Foglar are analogous art because they are from the same field of endeavor of ATM switching. At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify the previous combination of Shtayer and Foglar to verify that the non-selected bits are zeroed. The motivation for doing so would have been to detect and handle errors as suggested by Foglar in the passage from line 59 of column 8 through line 4 of column 9. Therefore, it would have been obvious to combine Foglar with Shtayer for the benefit of detecting and handling errors to obtain the invention as specified in claim 8.

Regarding claim **9**, Shtayer discloses the limitation of pre-selecting which bits are used to form the first address in lines 36-39 of column 5 which indicates that all bits are used to form the first address and that this is pre-determined.

Regarding claim **10**, Shtayer discloses the limitation of selecting each entry for the first memory in lines 33-61 of column 5 which describes how each field of each entry is selected.

Regarding claim **15**, Shtayer discloses the limitations of determine each entry within the first memory (see lines 33-61 of column 5 which describes how each field of each entry is selected); and determine which bits of a port number of a port that receives a data cell, a virtual path identifier for the data cell and a virtual channel identifier for the data cell are employed to generate an address for the first memory (see lines 36-39 of column 5 which indicates that all bits are used to form the first address and that this is pre-determined).

4. Claims **16-19** are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent 5,414,701 to Shtayer et al in view of U.S. Patent Application Publication 2010/0020802 to Willis.

Regarding claim **16**, Shtayer discloses a method for address mapping in a network processor, the method comprising: determining a port number of a port that receives a data cell (the PHY/LINK Id 14 of Figures 1, 3, and 5); determining a virtual path identifier and a virtual channel identifier for the data cell (see lines 64-68 of column 5 and lines 30-34 of column 6); creating a first index based on at least one of the port number, the virtual path identifier and the virtual channel identifier (the PHY/LINK Id is used to index the link table in Figures 3 and 5); accessing one of a plurality of entries stored in a first memory using the first index (the PHY/LINK Id is used to index the link table in Figures 3 and 5); creating a second index based

on the accessed entry of the first memory (see Figure 3 - the VP Index is created using the VP_MASK of the link table entry); and accessing an entry of a second memory based on the second index (see Figure 3 – the Link VP Table is accessed using this second index (VP Index)).

Shtayer does not disclose expressly the limitation that the first memory is an on-chip memory. However, consider Willis, which discloses a similar system for looking up routing information. As shown in Figure 19, the lookup information of Willis is structured so that a first set of entries (the PLUT and VPLUT entries) is stored on an ASIC (see the notation in Figure 19); that is, these entries are stored in an on-chip memory. These entries are used to access a second memory (the VCLUT entries of Figure 19). At the time of the invention, it would have been obvious to one of ordinary skill in the art to modify Shtayer to store the elements of the link table of Figure 3 on an on-chip memory. The rationale for doing so would have been to perform the lookups in the link table using faster on-chip memory and thereby speeding up the entire lookup operation; if the entire lookup operation accesses off-chip memory, it will generally be slower than an operation which uses some on-chip memory.

Similarly, regarding claim **18**, Shtayer discloses a system adapted to perform address mapping in a network processor comprising: a first memory having a plurality of entries (the link table of Figure 3); and a logic circuit adapted to: create a first index based on at least one of a number of a port that receives a data cell, a virtual path identifier for the data ceil and a virtual channel identifier for the data cell (the PHY/LINK Id is used to index the link table in Figures 3 and 5); access one of the plurality of entries stored in the first memory using the first index (see

lines 33-52 of column 5); and create a second index based on the accessed entry of the first memory (see Figure 3 – the VP Index is created using the VP_MASK of the link table entry).

Shtayer does not disclose expressly the limitation that the first memory is an on-chip memory. However, consider Willis, which discloses a similar system for looking up routing information. As shown in Figure 19, the lookup information of Willis is structured so that a first set of entries (the PLUT and VPLUT entries) is stored on an ASIC (see the notation in Figure 19); that is, these entries are stored in an on-chip memory. These entries are used to access a second memory (the VCLUT entries of Figure 19). At the time of the invention, it would have been obvious to one of ordinary skill in the art to modify Shtayer to store the elements of the link table of Figure 3 on an on-chip memory. The rationale for doing so would have been to perform the lookups in the link table using faster on-chip memory and thereby speeding up the entire lookup operation; if the entire lookup operation accesses off-chip memory, it will generally be slower than an operation which uses some on-chip memory.

Regarding claims **17 and 19**, Shtayer discloses the limitation that each entry stored in the first on-chip memory contains a base address field (the VP_POINTER field) and one or more of a number of port number bits field, a number of virtual path identifier bits field and a number of virtual channel identifier bits field (the VP_MASK field, as indicated in figure 4, indicates the number of VPI bits to be used).

5. Claim **4** is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 5,414,701 to Shtayer, et al in view of U.S. Patent 6,356,552 to Foglar and in further view of U.S. Patent 6,272,504 to Baentsch et al.

As disclosed above, the combination of Shtayer and Foglar discloses all limitations of parent claim 3 and thus the limitation of claim 4 that the first memory is on-chip. However, the combination of Shtayer and Foglar does not disclose expressly that the first memory comprises a random access memory. However, Baentsch discloses the advantage of random access memory in lines 8-10 of column 2. At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify Shtayer and Foglar to explicitly use random access memory (RAM) for the link table. The motivation for doing so would have been to provide faster memory access as suggested by Baentsch in lines 9-10 of column 2. Therefore, it would have been obvious to combine Baentsch with Shtayer and Foglar for the benefit of faster memory access to obtain the invention as specified in claim 4.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ROBERT C. SCHEIBEL whose telephone number is (571)272-3169. The examiner can normally be reached on Mon-Fri from 8:30 AM - 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Pankaj Kumar can be reached on 571-272-3011. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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